REMARKS

The enclosed is responsive to the Examiner's Final Office Action mailed on June 13, 2008, and is being filed pursuant to a Request for Continued Examination (RCE) as provided under 37 CFR 1.114. At the time the Examiner mailed the Final Office Action claims 19 and 20 were pending. By way of the present response the Applicants have: 1) amended claim 19; 2) added new claims 21-23; and 3) canceled no claims. As such, claims 19-23 are now pending. The Applicants respectfully request reconsideration of the present application and the allowance of all claims now represented.

Claim Rejections

35 U.S.C. 103(a) Rejections

The Examiner rejected claims 19 and 20 under 35 U.S.C. 103(a) as being unpatentable over Vogel, U.S. Patent 6,839,352 (hereinafter "Vogel") in view of Richards, et al., U.S. Patent 6,801,535 (hereinafter "Richards"). Applicants respectfully submit that the combination of Vogel and Richards does not describe what Applicants' claims require.

Vogel describes a "single-chip synchronous optical network (SONET) physical layer device [which] includes first, second and third interface ports." (Vogel, Abstract.) Vogel describes that a "UTOPIA interface block 42 ... generates ... header fields 12 for each of the ATM cells 10 based on the header field extracted from the PPP payload field." (Vogel, col.7 ll.44-48.)

Richards describes "[a] data reception unit for receiving plurality of data streams over a data channel..." (Richards, Abstract.) Richards describes the use of buffer memory (Fig. 8) from which "blocks of memory" can be assigned to each message channel. (*See* Richards, col.10 ll.20-22.) Additionally, a "free-list" of unassigned buffer blocks is maintainted." (*See* Richards, col.10 ll.45-49.)

With respect to claim 19, the combination of Vogel and Richards does not describe what Applicants are claiming. Specifically, the combination does not describe:

first circuitry to generate a packet based on header data received from a micro-engine and packet header data from a memory controller, the first circuitry comprising:

second circuitry to receive packet data from the memory controller, and to store the packet data in first-in first-out (FIFO) circuitry; and

third circuitry to track a start lane in the FIFO circuitry indicating a start of free space in the FIFO circuitry, and to determine a starting lane for packet payload such that alignment of payload data matches the start lane in the FIFO circuitry.

First, the combination does not describe "first circuitry to generate a packet based on header data received from a micro-engine and packet header data from a memory controller." The Office Action cites Vogel for this limitation. However, Vogel does not describe generating a packet, but only a packet header and not from data from a micro-engine or a memory controller.

Second, the combination does not describe "second circuitry to receive packet data from the memory controller, and to store the packet data in first-in first-out (FIFO) circuitry." Again, Vogel was cited for this limitation. Vogel does not describe the use of a memory controller much less receiving packet data from one.

Finally, the Office Action asserts that Richards' "free-list" (Fig. 10) describes "third circuitry to track a start lane in the FIFO circuitry indicating a start of free space in the FIFO circuitry, and to determine a starting lane for packet payload such that alignment of payload data matches the start lane in the FIFO circuitry." However, is nothing to suggest that this "free-list" is FIFO and its illustration actually depicts non-contiguous memory which highly suggests a non-FIFO buffer. Moreover, there is nothing in Richards' "free-list" that suggests determining a starting lane for packet payload such that alignment of payload data matches the start lane in the FIFO circuitry as there is no alignment of payload data, etc.

Thus, the combination does not describe what Applicants claim 19 requires. Claims 20-21 are dependent on claim 19 and are allowable for at least the same reason.

In light of the comments above, the Applicants respectfully request the allowance of all claims.

CONCLUSION

Applicant respectfully submits that all rejections have been overcome and that all pending claims are in condition for allowance.

If there are any additional charges, please charge them to our Deposit Account Number 02-2666. If a telephone conference would facilitate the prosecution of this application, the Examiner is invited to contact Dave Nicholson at (408) 720-8300.

Respectfully submitted,

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